RUTGERS
School of Engineering

Rutgers University
Electrical and Computer Engineering Department
14:332:436 Topics in ECE: VLSI Testing
`index 19291` **Spring 2015**

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Course Description: The physical challenges incurred by the rapidly shrinking feature size and reduced power supply voltage of deep sub-micron semiconductor fabrication technologies continue to give rise to various design robustness concerns. Due to the trend of increasing test costs, and the fact that test costs have started to dominate the overall production costs, low cost testing techniques and design-for-testability strategies have gained wide attention. This course covers the problems of testing of Very Large Scale Integrates Circuits (VLSI), the design of circuits for testability, design of Built-In-Self-Test circuits (BIST), and use of IEEE Boundary Scan standards. The aim of this course is to educate the students to understand the fundamentals of VLSI testing strategies and design-for-testability techniques that are currently used in high-technology industries.

Prerequisites:

- 14:332:331: Computer Architecture and Assembly Language
- Senior Standing required

Text book: "Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits", M. L. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2005.

Tool used in this course:

- Synopsys TetraMax

Course Syllabus:

- **Introduction to testing**
  - Types of testing
  - Test economic
- **Fault modeling**
  - Permanent faults
  - Transition faults
  - Fault equivalence

- Fault dominance

- **Logic and fault simulation**
  - True-value simulation
    - Compiled-code simulation
    - Event-driven simulation
  - Fault simulation
    - Serial fault simulation
    - Parallel fault simulation
    - Deductive fault simulation
    - Concurrent fault simulation
- **Testability measures**
  - Controllability and observability measurement
- **Combinational Automatic Test Pattern Generation (ATPG)**
  - Functional vs. structural ATPG
  - D-algorithm
  - PODEM
- **Sequential ATPG**
  - Time-frame expansion
- **Delay-Fault testing**
  - Transition-delay testing
    - Launch-on-Capture scheme (LoC)
    - Launch-on-Shift scheme (LoS)
  - Path-delay testing
- **Design For Testability (DFT)**
  - Scan design
    - Full-scan design
    - Partial-scan design
  - Built-In Self Test (BIST)
    - BIST pattern generation (PG)
    - BIST response compaction (RC)
  - Boundary scan
- **Test set compaction / compression**
  - Test-stimulus compression
  - Test-response compaction
- **Memory testing**
- **SoC testing**